Semiconductor Devices - 2014

Lecture Course
Part of
SS Module PY4P03

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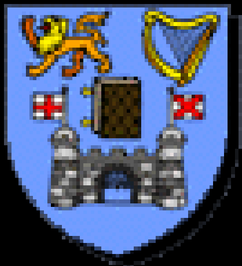
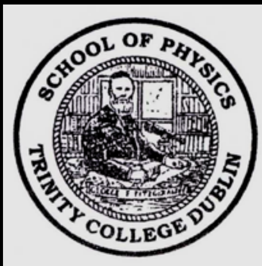


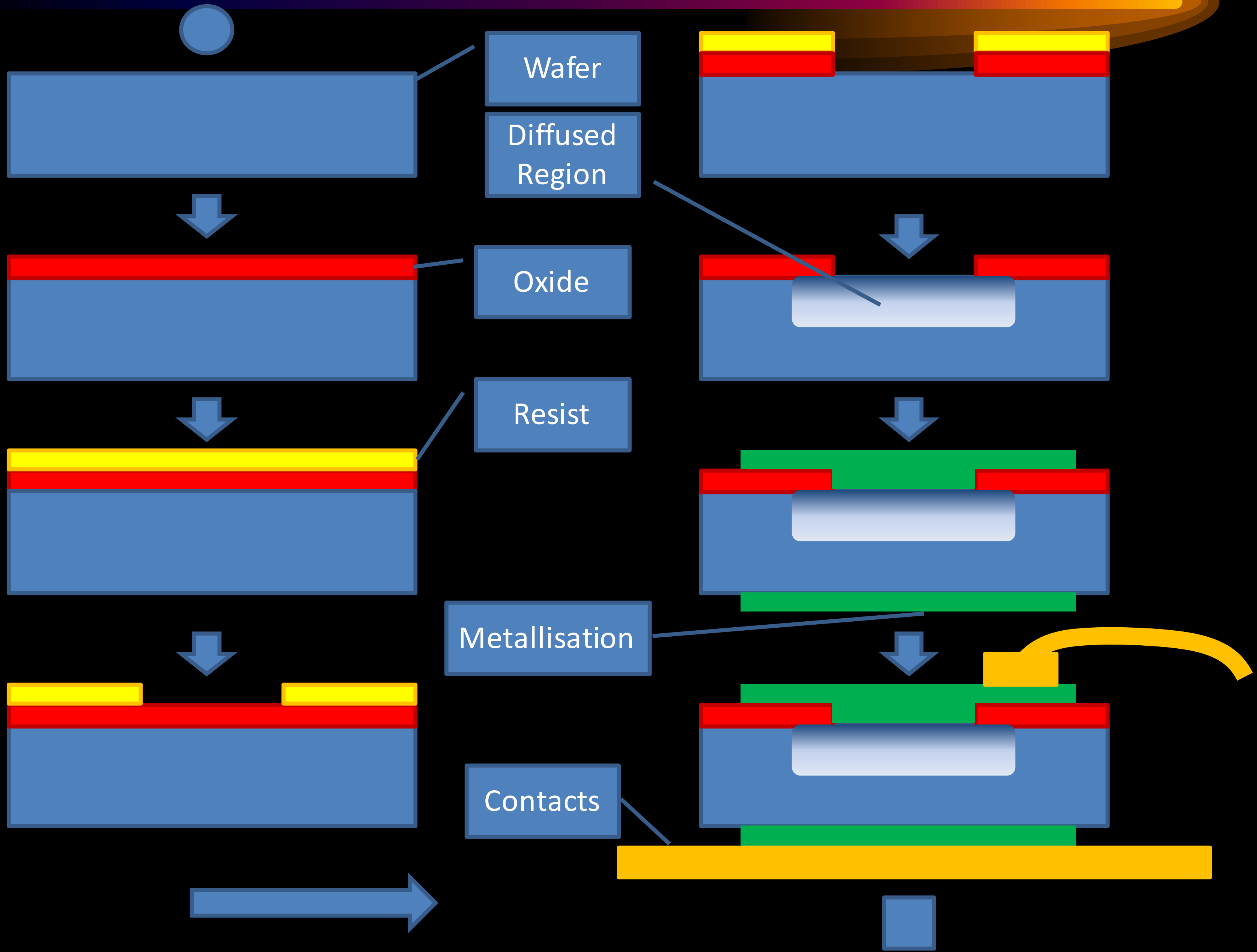


Hilary Term, TCD
31th of Feb '14

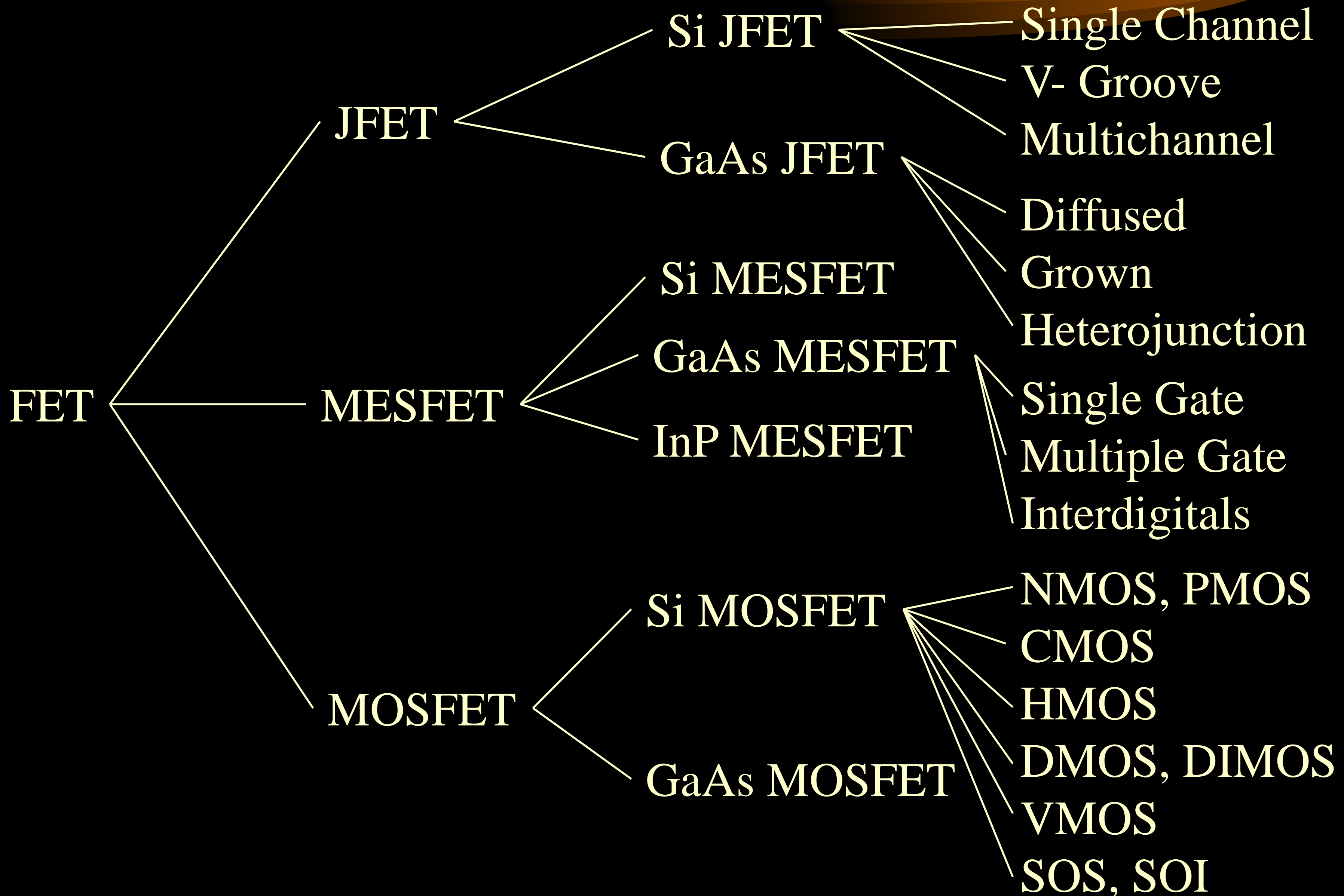
Overview of JFETs and MOSFETs

- Realistic fabrication (process flow example)
- The FET Family Tree
- FET Structures
- JFET Modelling
- MOSFET Modelling

Process Flow Example – p-n Diode



Unipolar FETs' Family Free



Remarks on FETs

- Essentially unipolar devices – the current flow (either holes or electrons) between two electrodes (source and drain) is controlled by the potential difference to a third electrode (gate).
- Close (closer) to ohmic behaviour. Linear or square law. Lower total harmonic distortion and intermodulation distortion.
- Much higher input impedance. Lower input currents. Simpler matching to microwave circuits.
- Negative temperature coefficient. Self-limiting, with a much lower probability for a thermal runaway or breakdown.
- No minority carrier storage effects – higher switching speeds and higher cutoff frequencies.
- Conceptually simpler, with close to equilibrium carrier concentrations, virtually no carrier injection or extraction.
- Could have been the first ones to be realized...

Jan. 28, 1930. J. E. LILIENFELD 1,745,175

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

Filed Oct. 8, 1926

Fig. 1.

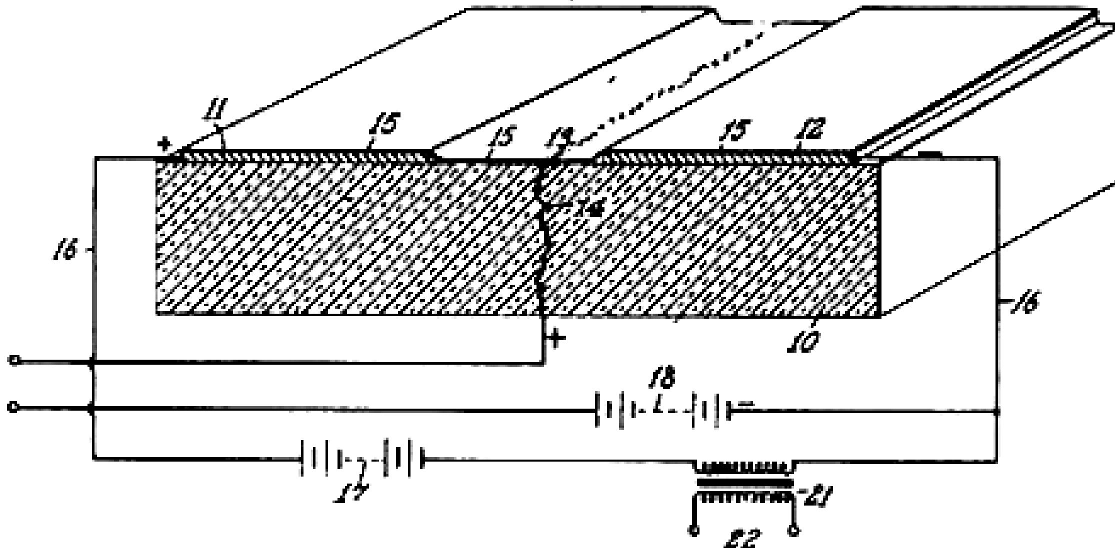
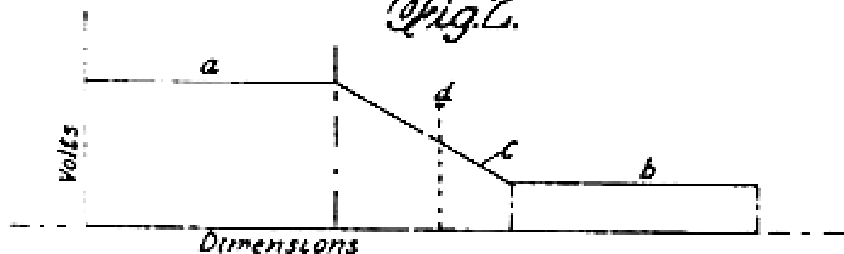


Fig. 2.

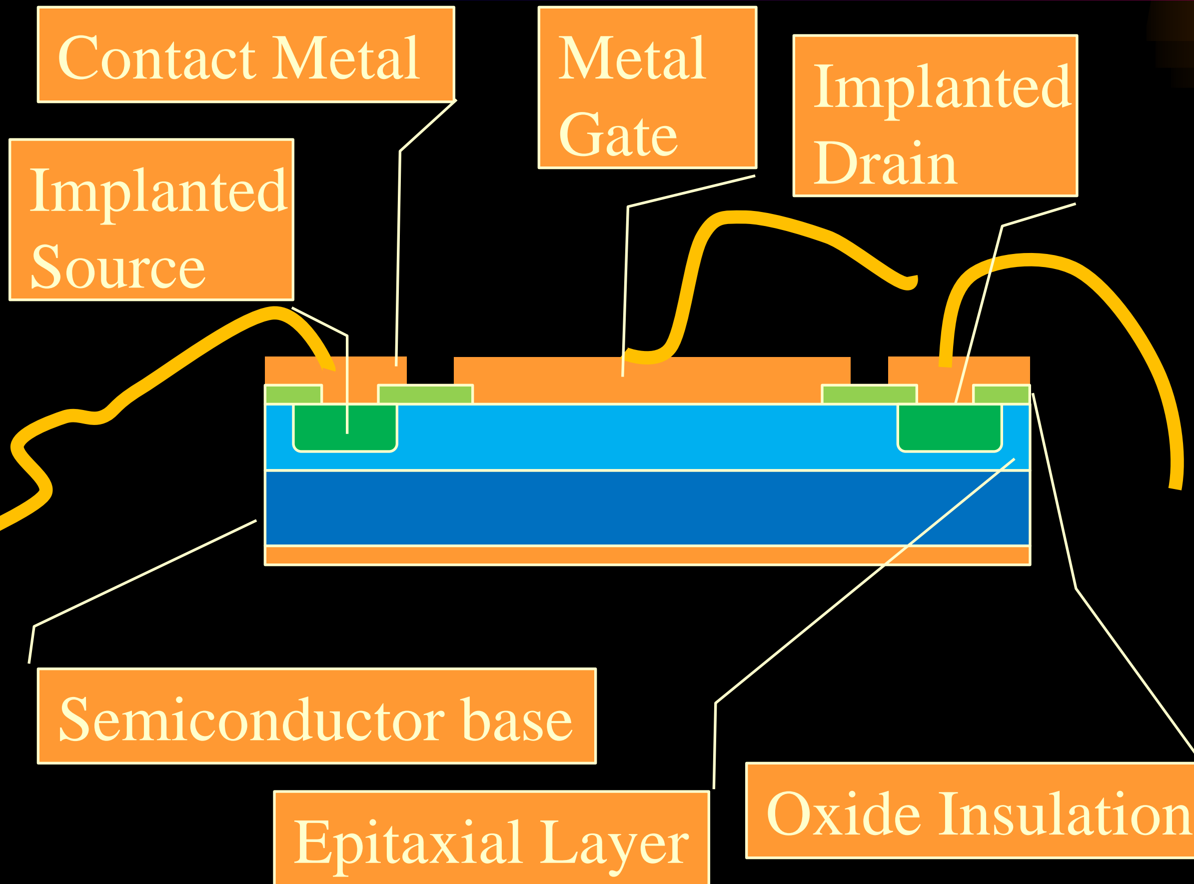


INVENTOR
Julius Edgar Lilienfeld
BY
ATTORNEY

..The First One

- Part of Lilienfeld's first patent. This resembles a modern MESFET, but was unrealisable without semiconductors.
- Shockley *et al* ~ 1948 worked on similar concepts, but had to abandon patenting them because of Lilienfeld's work. Reproposed by Mead *et al* ~1966
- Most semiconductor transistors are now unipolar.

MEtal Semiconductor - MESFET



- Relatively simple – can work with compound semiconductors (Schottky gate)
- Fast – can use high mobility channels
- Can be done in SOI version, as well

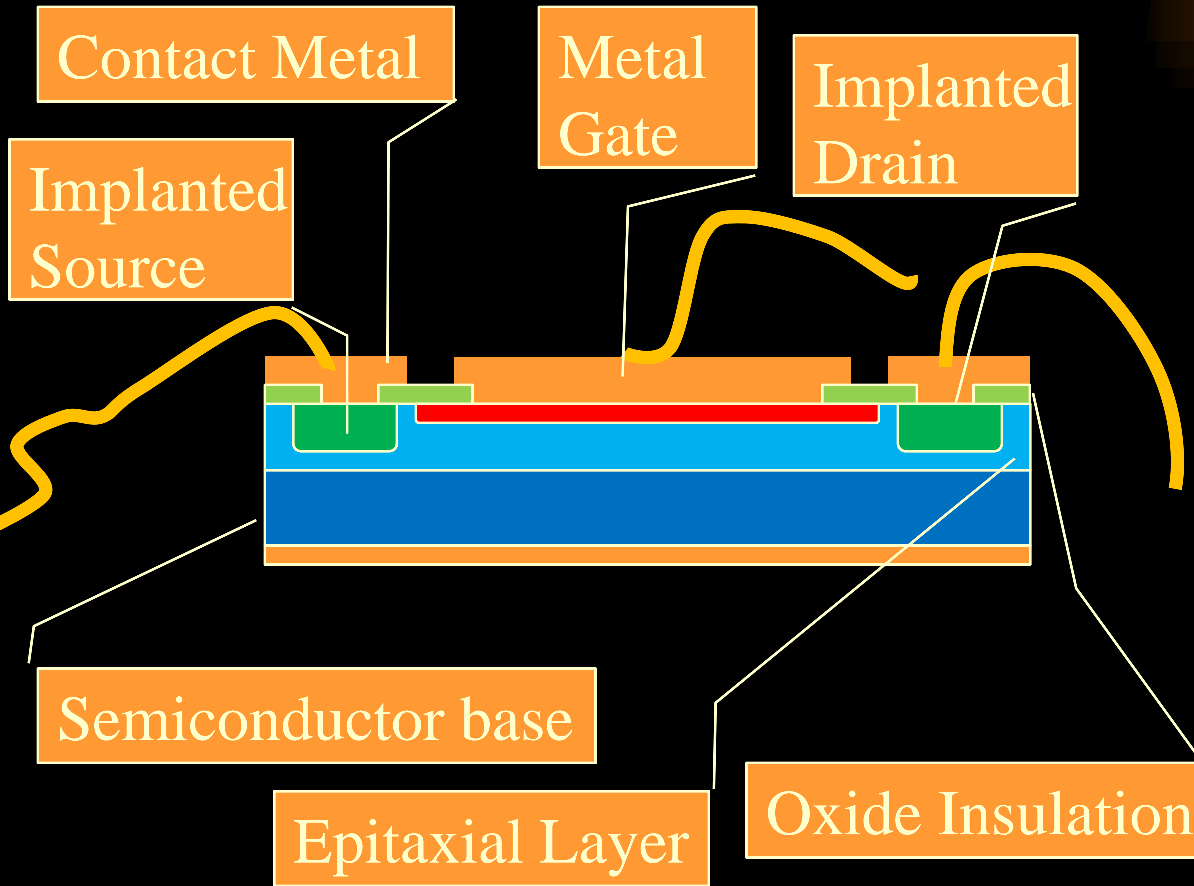
Recipe

- ...
- Grow an epilayer
- Oxidize
- Open windows
- Implant
- Metalize
- ...

Features

- Building block
- Provides gain
- Voltage-control device
- Unipolar device

Junction Field Effect Transistor - JFET



Recipe

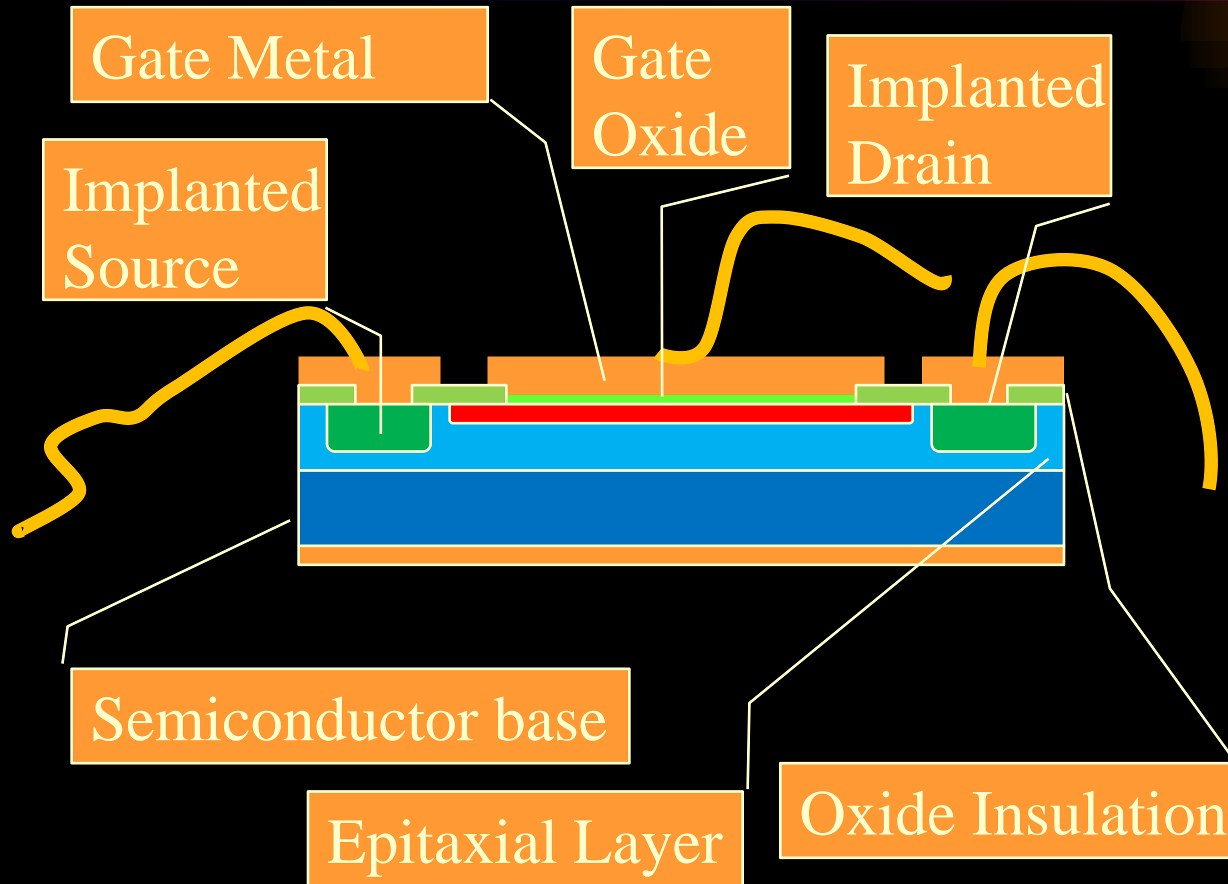
- ...
- Grow an epilayer
- Oxidize
- Open windows
- Diffuse junction
- Metalize
- ...

Features

- Building block
- Provides gain
- Voltage-control device
- Unipolar device

- Low noise – finite gate current
- Very flexible intermediate frequencies amplifier (used widely in preamps)
- Enhancement and depletion modes

Metal Oxide Semiconductor - MOSFET



Recipe

- ...
- Grow an epilayer
- Oxidize
- Open windows
- Form gate oxide
- Metalize
- ...

Features

- Building block
- Provides gain
- Voltage-control device
- Unipolar device

- Very low gate current, but somewhat noisy
- Can use both bias signs at the gate contact
- Enhancement and depletion modes
- Buried channel devices possible

Idealised JFET

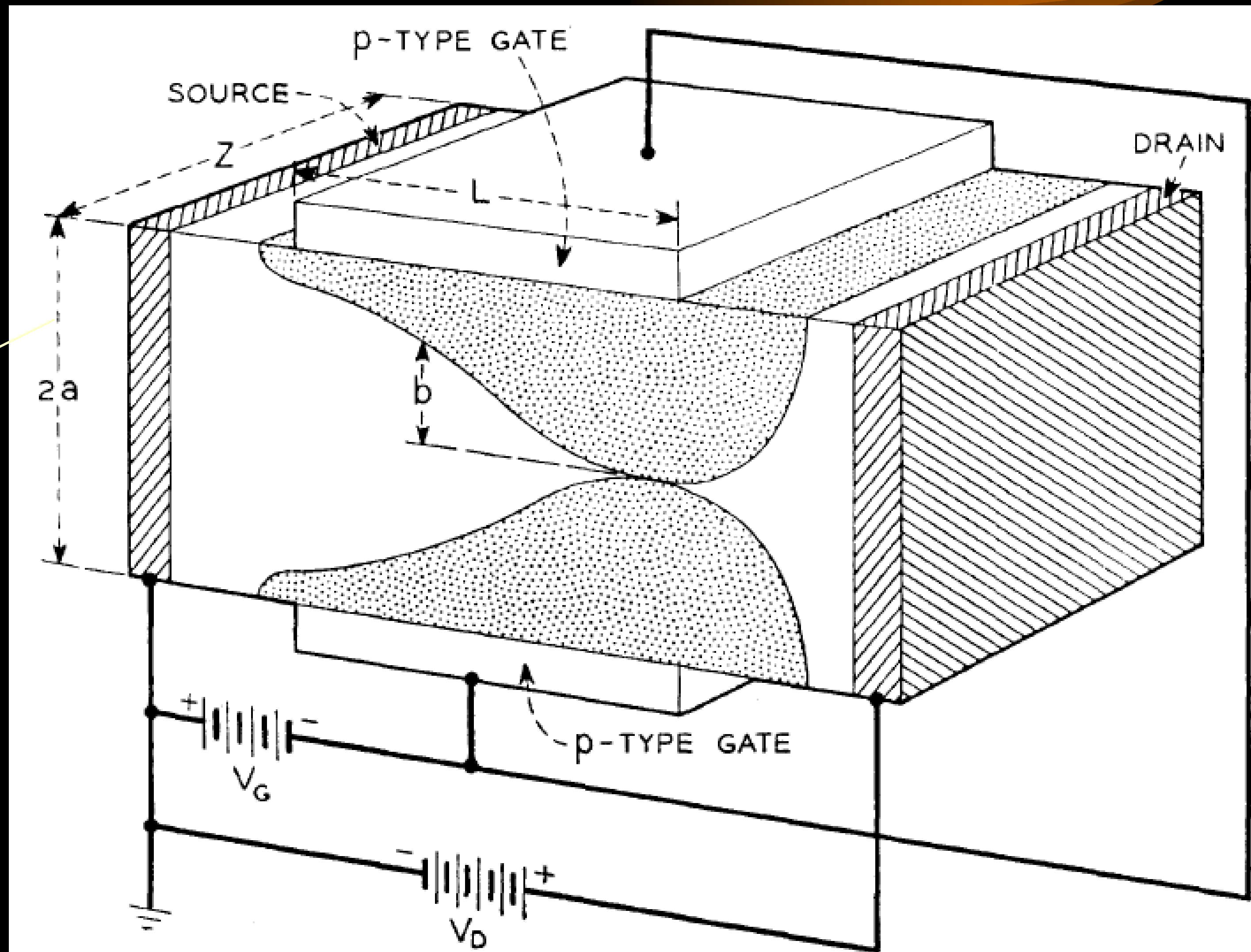


Fig. 1—Schematic diagram of field-effect transistor.

After:
G. C. Dacey
and I. M. Ross,
Proc. I. R. E.
41, 970 (1953)

Potential Distribution - JFET

$$-\frac{\partial^2 \phi(x)}{\partial y^2} = \frac{\rho(y)}{\epsilon_s}$$

Poisson's Equation for the channel

Threat as in diodes

$$-\frac{\partial^2 \phi(x)}{\partial y^2} = \frac{qN_d(x)}{\epsilon_s}$$

For *n*-type channel

$$\lambda_d(0) = \sqrt{\frac{2\epsilon_s\left[V_g + V_{bi}\right]}{qN_d}}$$

Depletion depth at source

Preparing for a purely linear approximation

$$\lambda_d(x) = \sqrt{\frac{2\epsilon_s\left[\phi(x) + V_g + V_{bi}\right]}{qN_d}}$$

Depletion depth at arb. position

$$V_{bi} = V_t \ln\left(\frac{N_d}{n_i}\right)$$

Build-in potential

Drain Current - JFET

$$\lambda_d(L) = \sqrt{\frac{2\epsilon_s [V_d + V_g + V_{bi}]}{qN_d}}$$

Depletion depth at drain

At the opposite end of the gate

$$V_p = V_d[\lambda_d(L) = a] = \frac{qN_d a^2}{2\epsilon_s}$$

Pinch-off Voltage

Drude's law

$$J_x(y) = \sigma(x)\mathcal{E}_x(y) = -qN_d\mu \frac{\partial \phi(x,y)}{\partial x}$$

Current Density

$$I_d = \frac{1}{L}\int_{\lambda_d(0)}^{\lambda_d(L)} d\lambda_d qN_d\mu \frac{\partial \phi(x)}{\partial x}[a - \lambda_d(x)]Z$$

Drain Current

Remember that λ_d is variable in the channel

$$\frac{\partial \phi(x)}{\partial \lambda_d} = \frac{qN_D}{\epsilon_s}\lambda_d$$

Potential variation in the channel

Saturation Current - JFET

$$I_\mathrm{d} = \frac{Z\mu q^2 N_\mathrm{d}^2 a^3}{6\epsilon_\mathrm{s} L}\left\{\frac{3}{a^2}\left[\lambda_\mathrm{d}^2(L) - \lambda_\mathrm{d}^2(0)\right] - \frac{2}{a^3}\left[\lambda_\mathrm{d}^3(L) - \lambda_\mathrm{d}^3(0)\right]\right\}$$

Pinch-off currenr

$$I_\mathrm{p} = \frac{Z\mu q^2 N_\mathrm{d}^2 a^3}{6\epsilon_\mathrm{s} L}$$

Drain Current

$$I_\mathrm{d}^\mathrm{sat} = I_\mathrm{p}\left[1 - 3\left(\frac{V_\mathrm{g} + V_\mathrm{bi}}{V_\mathrm{p}}\right) + 2\left(\frac{V_\mathrm{g} + V_\mathrm{bi}}{V_\mathrm{p}}\right)^{3/2}\right]$$

Saturation Bias

$$V_\mathrm{d}^\mathrm{sat} = V_\mathrm{p} - V_\mathrm{g} - V_\mathrm{bi}$$

Saturation Current

$$g_\mathrm{max} = qN_\mathrm{d}\mu\frac{aZ}{L}$$

$$g_\mathrm{m} = \frac{\partial I_\mathrm{d}}{\partial V_\mathrm{g}}$$

$$g_\mathrm{d} = \frac{\partial I_\mathrm{d}}{\partial V_\mathrm{d}}$$

Transconductances

Transconductance and Drain Current

$$g_{\mathrm{d}}(V_{\mathrm{d}} \to 0) \approx g_{\max}\left(1 - \sqrt{\frac{V_{\mathrm{g}} + V_{\mathrm{bi}}}{V_{\mathrm{p}}}}\right)$$

Drain Conductance

$$g_{\mathrm{m}}^{\mathrm{sat}} \approx g_{\max}\left(1 - \sqrt{\frac{V_{\mathrm{g}} + V_{\mathrm{bi}}}{V_{\mathrm{p}}}}\right)$$

Gate Transconductance

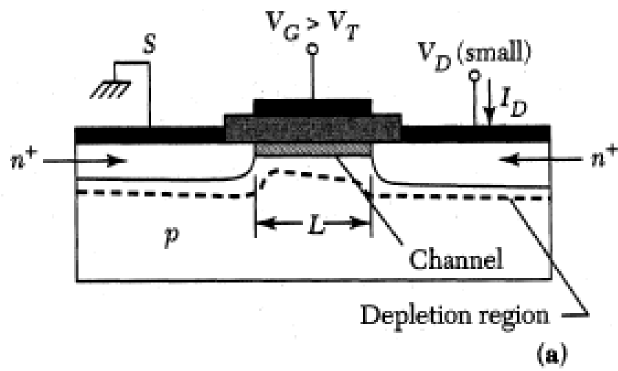
$$V_{\mathrm{th}} \simeq V_{\mathrm{bi}} - V_{\mathrm{p}}$$

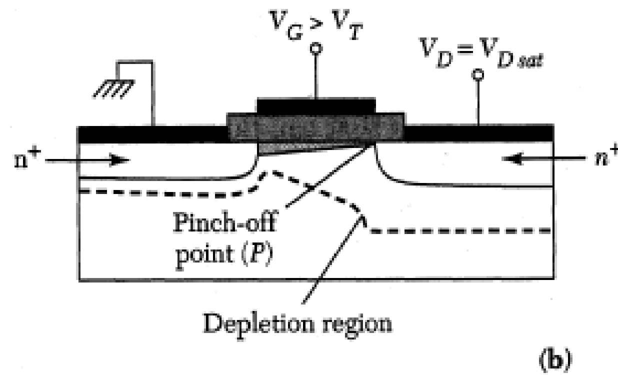
Threshold Voltage

$$I_{\mathrm{d}} \approx \frac{\mu \epsilon_{\mathrm{s}} Z}{2aL}\left(V_{\mathrm{g}} - V_{\mathrm{th}}\right)^{2}$$

Approximate Drain Current Expression. REMEMBER!

The MOSFET





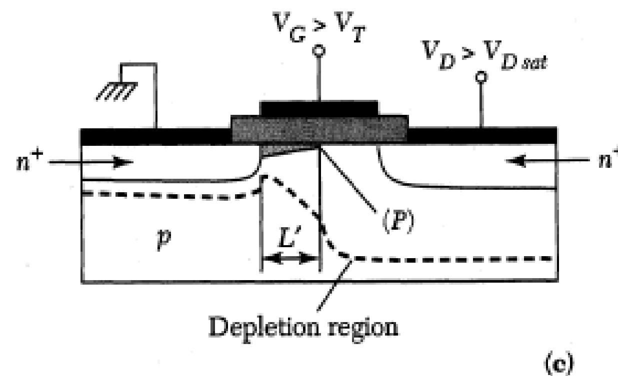


Fig. 15 Operations of the MOSFET and output *I-V* characteristics. (*a*) Low drain voltage. (*b*) Onset of saturation. Point *P* indicates the pinch-off point. (*c*) Beyond saturation.

After: S. M. Sze, Physics of Semiconductor Devices, 2nd edition

Conductivity – MOSFET case

$$\sigma(y) = qn(y)\mu(y)$$

Conductivity

$$g = \frac{Z}{L}\int_0^{y_i} \sigma(y)\mathrm{d}y$$

Conductance

$$g = \frac{qZ\mu}{L}\int_0^{y_i} n(y)\mathrm{d}y = q\mu\frac{Z}{L}\left|Q_n\right|$$

$$\mathrm{d}\psi = I_d \mathrm{d}R = I_d \frac{1}{gL}\mathrm{d}x = \frac{I_d}{Z\mu\left|Q_n(x)\right|}\mathrm{d}x$$

Potential Distribution

$$V_d = \int_0^{\psi(L)} \mathrm{d}\psi = \frac{I_d}{Z\mu}\int_0^{L} \frac{1}{\left|Q_n(x)\right|}\mathrm{d}x$$

Drain Voltage

Charge Distribution in the Channel

$$Q_{\mathrm{n}}(x) = -\left[V_{\mathrm{g}} - \psi(x) - 2\psi_{\mathrm{b}}\right] C_{\mathrm{i}} + \sqrt{2\epsilon_{\mathrm{s}} q N_{\mathrm{a}} \left[\psi(x) + 2\psi_{\mathrm{b}}\right]}$$

Distributed Charge

Intrinsic Capacitance

$$C_{\mathrm{i}} = \frac{\epsilon_{\mathrm{i}}}{d} \approx \frac{\epsilon_{\mathrm{s}}}{d}$$

$$I_{\mathrm{d}} = \frac{Z}{L}\mu C_{\mathrm{i}} \left\{ \left(V_{\mathrm{g}} - 2\psi_{\mathrm{b}} - \frac{V_{\mathrm{d}}}{2} \right) V_{\mathrm{d}} - \ldots \right\}$$

Drain Current

$$V_{\mathrm{th}} = 2\psi_{\mathrm{b}} + \frac{\sqrt{2\epsilon_{\mathrm{s}} q N_{\mathrm{a}} (2\psi_{\mathrm{b}})}}{C_{\mathrm{i}}}$$

Threshold Voltage

$$I_{\mathrm{d}} \simeq \frac{Z}{L}\mu C_{\mathrm{i}} \left(V_{\mathrm{g}} - V_{\mathrm{th}}\right) V_{\mathrm{d}}$$

Approximate Expression REMEMBER!

Thank You Very Much for Your Attention!