

PY2N20

**Material Properties and
Phase Diagrams**

Lecture 9

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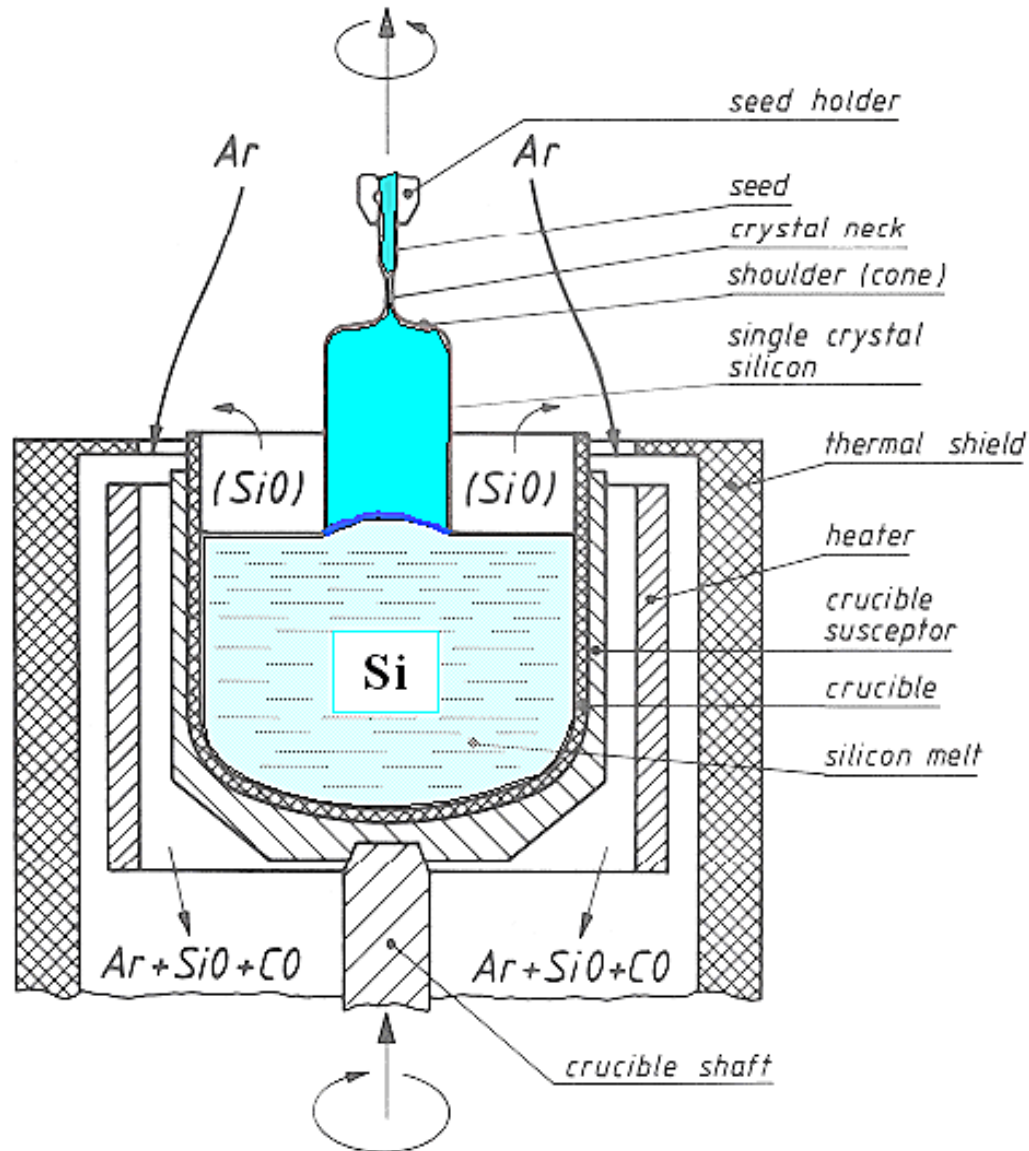
Semiconductor Wafer Production - Si

Czochralski Growth

- Growth from melt
- Melt 99.999999% pure polycrystalline Si (Think about the methods necessary to reliably characterize this level of impurity concentration!)
- Quartz or Graphite crucible (With a number of different implications.)
- Back filled with an inert gas (Argon)
- Heated to > 1414 °C, but < 1500 °C
- 'Pulling' of the crystal
- End result could have < 1 dislocation / m^2

Czochralski Growth

Beginning of crystal growth



Czochralski Growth

- Small 'seed' crystal – rotated in opposite sense to crucible
- Can pull a 'boule' of dimensions up to $\text{Ø}300 \text{ mm} \times 2000 \text{ mm}$ (450 mm on the way)
- Speed of pull determines e.g. defects
 - Fast pull initially \rightarrow because large temperature gradient \rightarrow high defect density \rightarrow don't want defects to propagate into boule \rightarrow causes 'necking'
 - Constant rate of pull setups
 - Use of high magnetic fields
 - Final length and mass (up to 1000 kg)

Czochralski Growth

- Must conduct **latent heat of freezing** away from solid/melt interface
- Rate of conduction of heat determines maximum speed
- Heat balance

$$V \rho L = K_s \frac{dT}{dx}$$

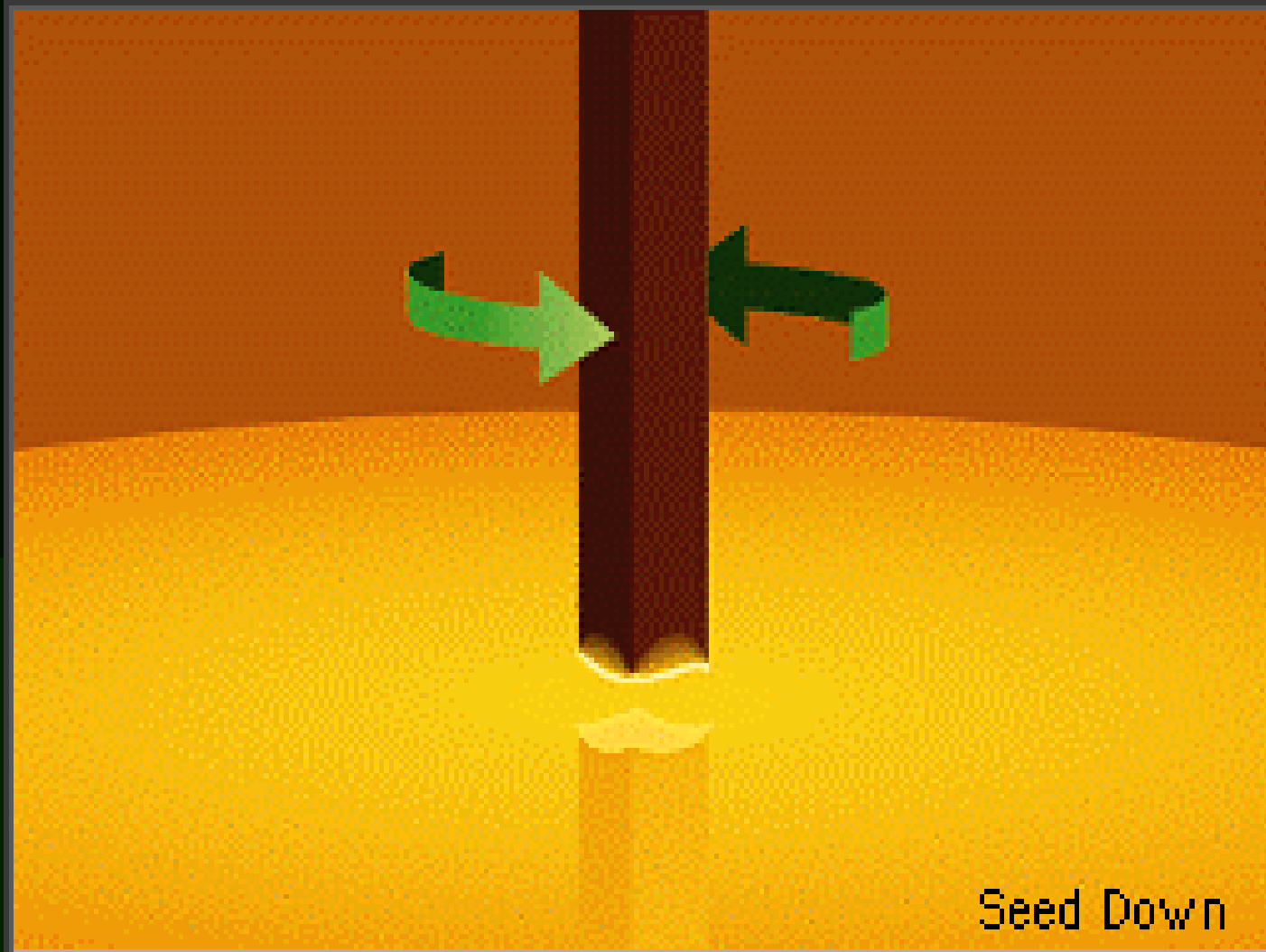
V = Rate of growth of crystal

ρ = density of Si

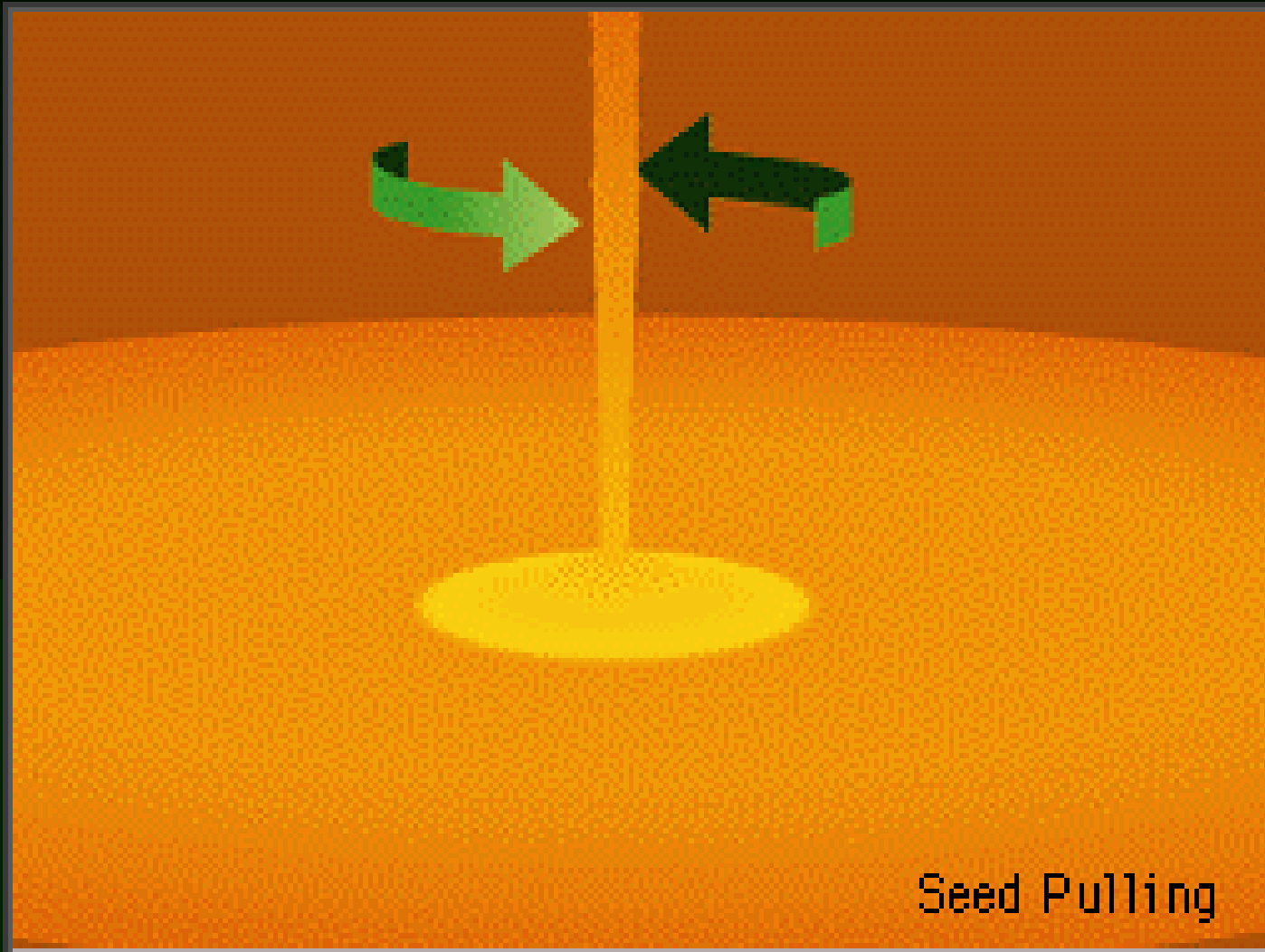
L = latent heat of freezing

K_s = Thermal conductivity

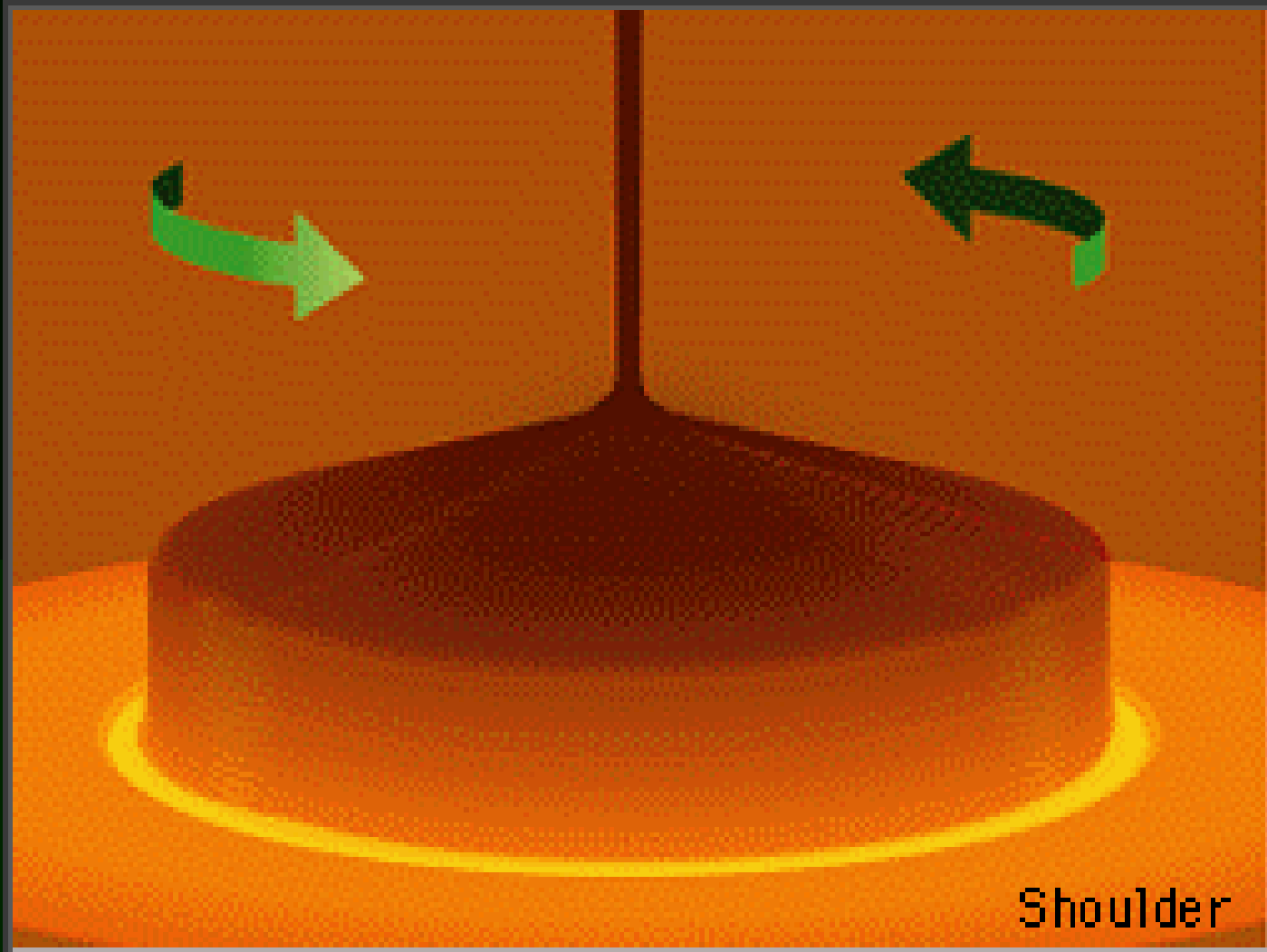
Czochralski Growth



Czochralski Growth



Czochralski Growth



Czochralski Growth

Main Contaminant – Oxygen from crucible

3 main effects

- **Oxygen is a dopant for Si**
 - **SiO₄ complexes formed**
- **Solution strengthening**
 - **Reduction in plastic deformation as the boule is withdrawn and cooled**
- **Oxygen precipitation**
 - **Increased dislocations**
 - **Problems with strain control**
 - **Mobility decrease**

Czochralski Growth

- Other impurities
- Carbon – as low as possible from outer crucible
- 3d metals – mobility (< 1 ppb) – ‘leached’ from the graphite
- Purpose doping
 - n - type: P, As, Sb
 - p - type: B, (Al and In used primarily for contacting)

Distribution of Impurities in Czochralski Growth

- Impurities have different free energies in melt and solid
 - Therefore the impurities 'partition'
 - Equilibrium partition coefficient, k is

$$k = \frac{I_S}{I_M}$$

where I_S and I_M are impurity concentrations in solid and melt.

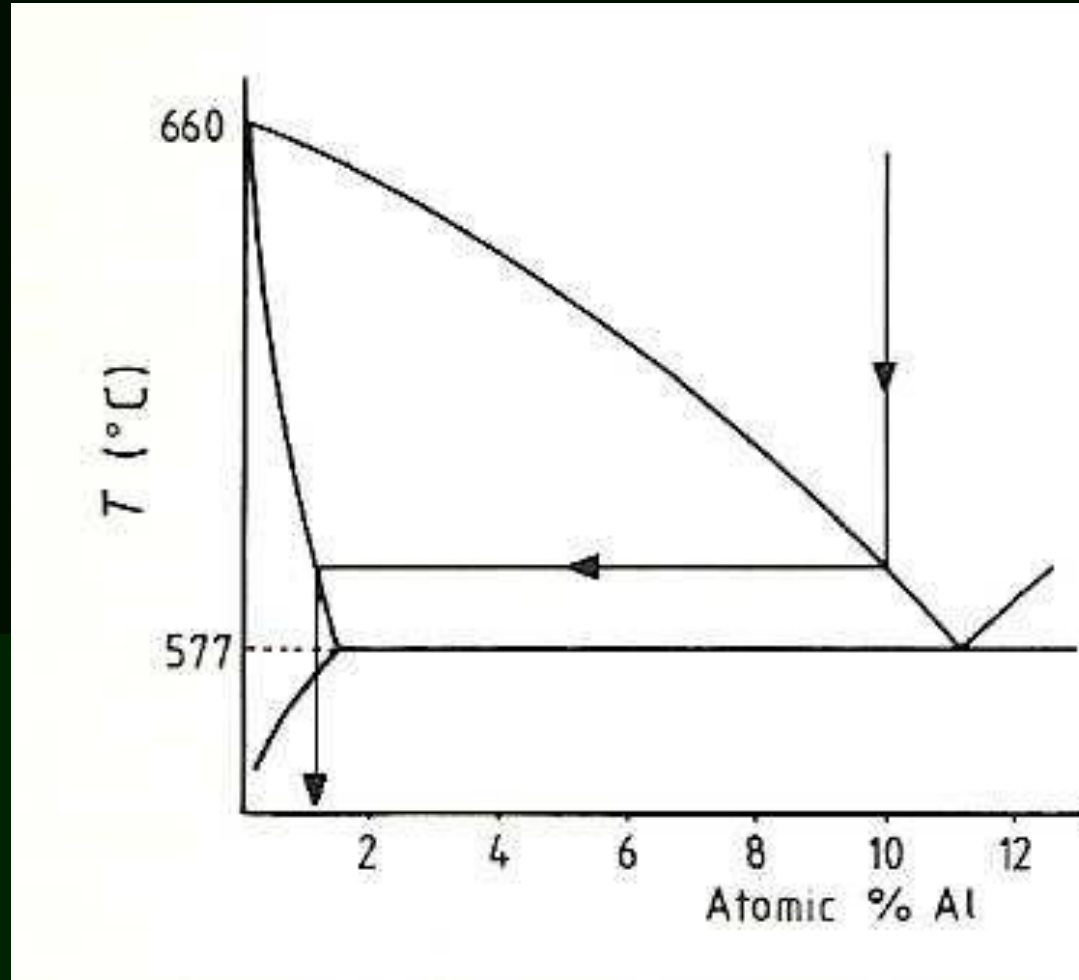
- Molten-zone refinement, zone melting, floating zone methods

Example 10% at. Al in Si

$$I_M = 10\%$$

$$I_S = 1\%$$

$$k = 0.1$$



Note: Data in this phase diagram is incorrect – shown for illustration purposes only!

Non-equilibrium case

- Effective partition coefficient estimated by

$$k_{eff} = \left[1 - \left(\frac{1}{k_0} - 1 \right) e^{\left(\frac{V\delta}{D} \right)} \right]^{-1}$$

k_0 = Equilibrium partition coefficient

δ = Boundary layer thickness

D = Diffusion rate in melt

V = rate of propagation

Effective Partition Coefficients

Table 3.2 Some measured values of partition coefficients for common impurities in semiconductors.

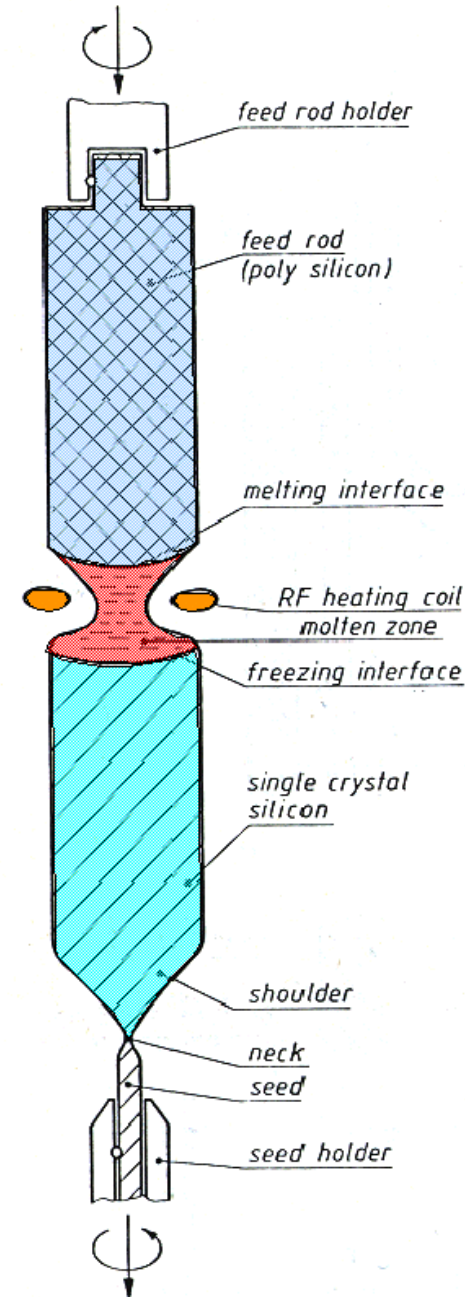
Silicon Impurity	Fe	Cu	Al	C	As	P	B	O
k_{eff}	0.000 006	0.0004	0.002	0.07	0.3	0.35–0.56	0.8	1.25
Gallium arsenide Impurity	Cu	Fe	Sn	In	Si	C	P	Al
k_{eff}	0.000 015	0.003	0.003–0.03	0.1	0.1	0.8	2	3
Indium phosphide Impurity	Ge	Sn	Te	Se	S			
k_{eff}	0.01	0.002–0.03	0.4	0.6	0.8			
Gallium phosphide Impurity	Sn	O	Zn					
k_{eff}	0.0001	0.005	0.05–0.08					

Note the difference for Al in Si

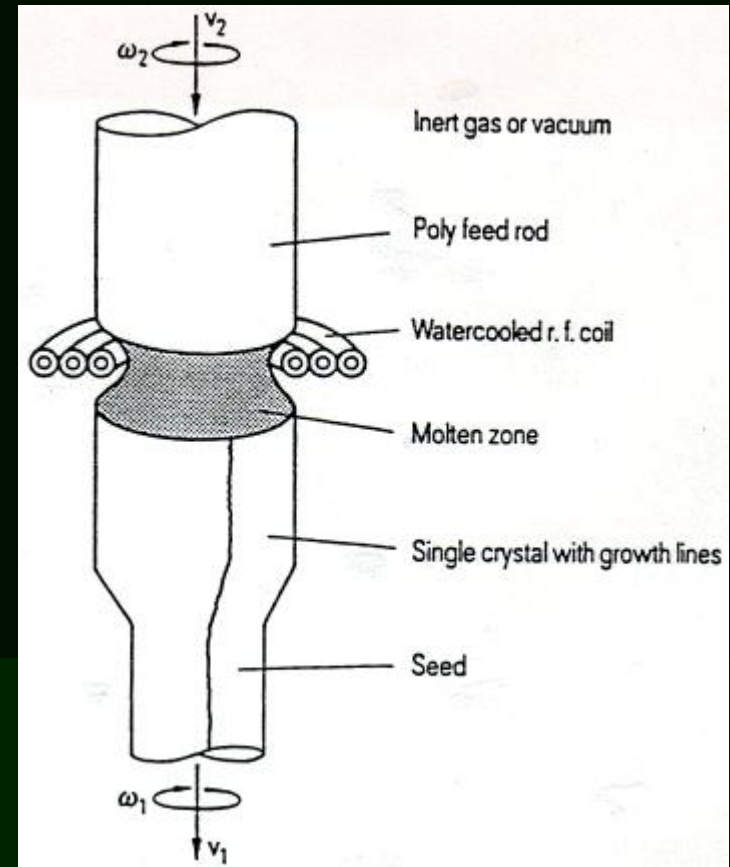
Float zone pulling

- Crucibleless process – at least in the vertical version
- Important for Ge (HPGe)
- Important for Solar Cell applications (carrier lifetime)
- Can be used with continuous feeding
- Variety of indirect heating options – inductive, radiative, plasma, or electron bombardment

Float-zone pulling



Molten Zone Refinement

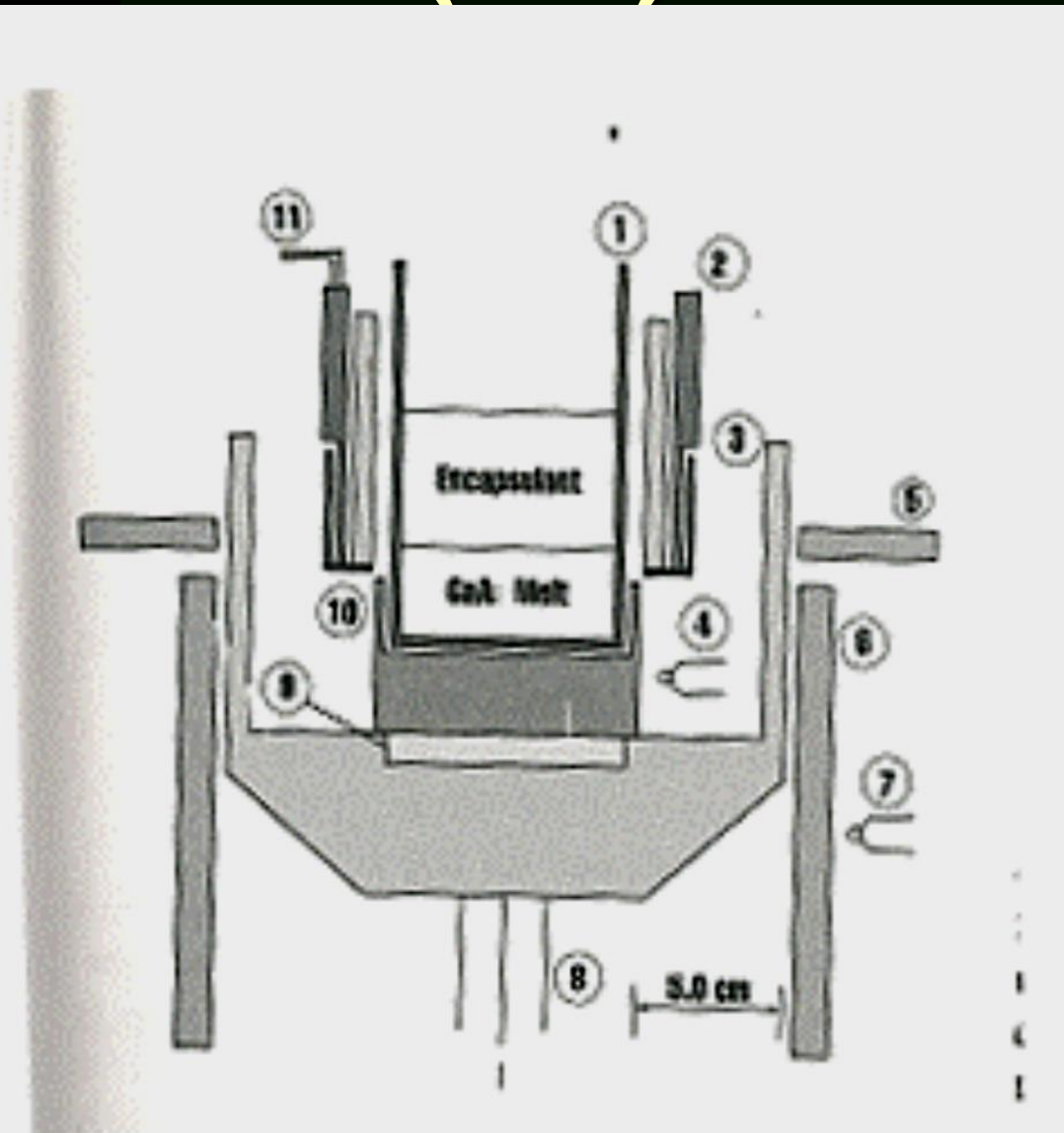


Better but more expensive.
Used when necessary.

Growth of *III-V* Semiconductors

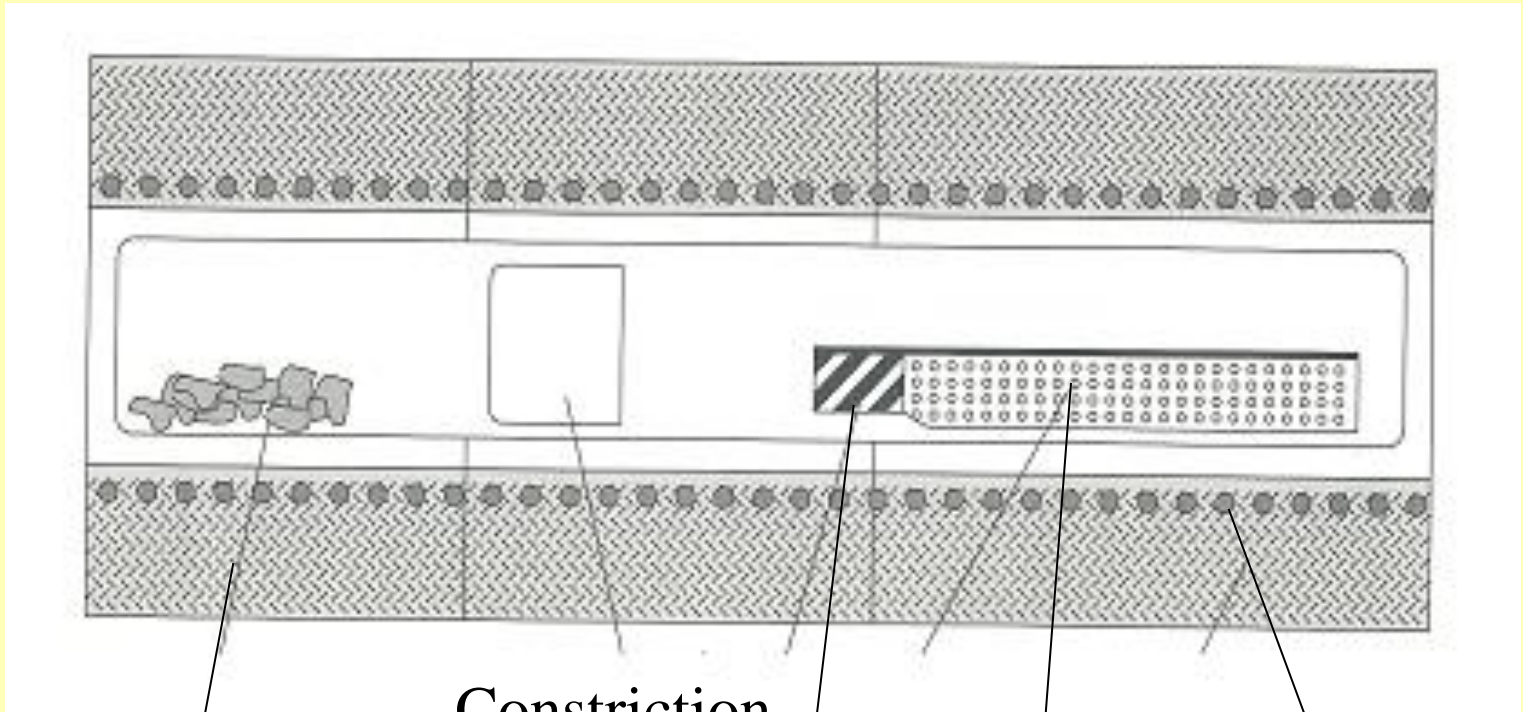
- Czochralski growth is problematic
 - Vapour pressure difference
 - As – ca. 0.9 atm
 - Ga – ca. 0.001 atm
 - Necessity to provide counter-pressure or use flux encapsulation
 - As is lost from the melt and stoichiometry is affected
 - Thermal conductivity of GaAs is about 33% that of Si → slower pull rate

Liquid Encapsulated Czochralski Growth (LEC)



(1) quartz crystal, (2) heat flux control system, (3) graphite shield, (4) cavity thermocouple, (5) radiation shield, (6) heater, (7) temperature control thermocouple, (8) water cooled support (9) insulation support, (10) graphite crucible support and (11) tubing support.

Bridgeman Process



As lumps as solid source

Constriction

GaAs seed

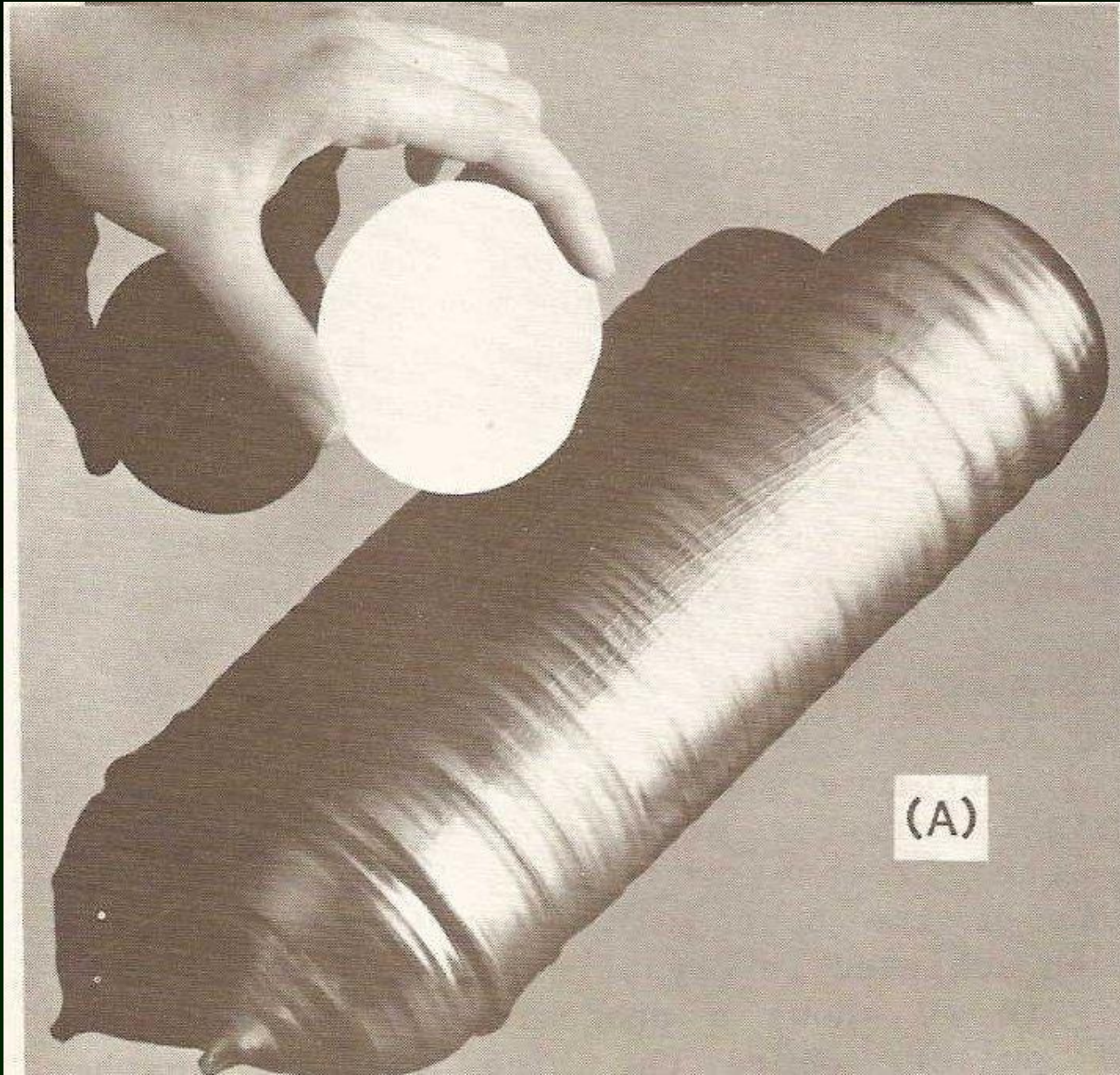
GaAs melt

Multi zone furnace

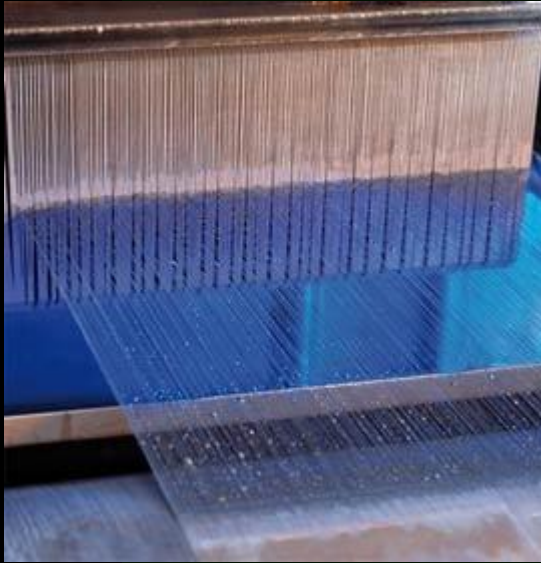
Bridgeman Process

- Advantages
 - Low defect density
 - Can be used for binary and ternary systems
- Disadvantages
 - D-shaped crystals
 - Slow growth rate 10 mm / hour

Boules and Ingots to Wafers



Cutting and Lapping



<http://www.solarserver.com>

Modern devices are created
'on-the-surface' ... and perfect surface
is very important...

Wafer from Boule

- Seed and tail removed
 - Grading
 - Cutting
- Trimmed to final diameter
 - Grinding
 - Etching
- 'Flat' ground along entire length
 - Orientation
 - Conductivity testing

Wafer Preparation

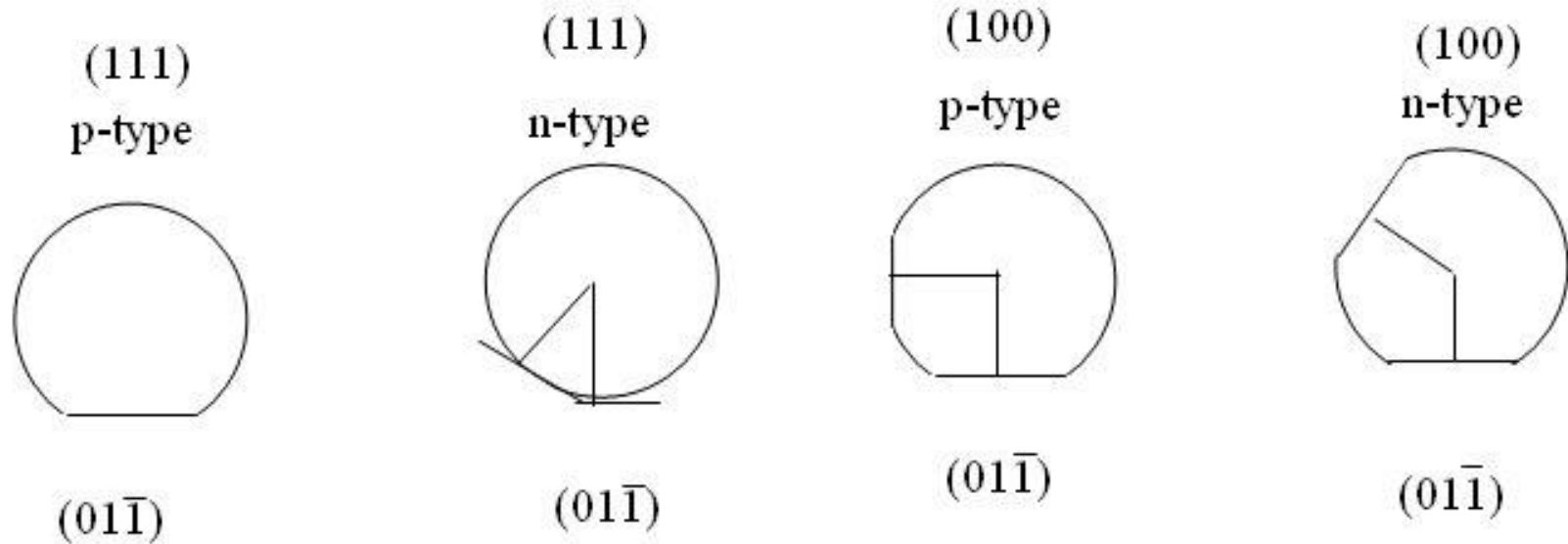
- An 'orientation' flat or groove is machined in the ingot – four point conductivity and other testing and quality grading is performed.
- Wafer blanks are sliced – usually using diamond wire saws. Thicknesses vary from about 0.3 mm for the small wafer sizes (1 inch) to about 0.8 mm for the largest sizes (12 inch).
- The blanks are polished first mechanically – 'lapped' with diamond paste to better than 3 μm tolerance.
- Combination of diffusion-controlled oxidation and diffusion-controlled etching (typically buffered HF + AF solution) until the wafers are close to atomically smooth.
- Oxidation and preparation of Silicon on Insulator (SOI), if required.
- The wafers are ready for device manufacturing

- About 100,000 metric tonnes of pure silicon are produced annually, but less than half of that is monocrystalline – the rest is destined for solar cell manufacturing.

Si (Standard) Wafer Sizes

- 1 inch.
- 2 inch (50.8 mm). Thickness 275 μm .
- 3 inch (76.2 mm). Thickness 375 μm .
- 4 inch (100 mm). Thickness 525 μm .
- 5 inch (127 mm) or 125 mm (4.9 inch). Thickness 625 μm .
- 150 mm (5.9 inch, usually referred to as "6 inch"). Thickness 675 μm .
- 200 mm (7.9 inch, usually referred to as "8 inch"). Thickness 725 μm .
- 300 mm (11.8 inch, usually referred to as "12 inch"). Thickness 775 μm .
- 450 mm ("18 inch"). Thickness 925 μm (expected).

Flat Orientations



Flat orientations for Si wafers

Above 200 mm – Orientation notches only – no flats!

Final Processing into wafers

- Etch in HF-HNO₃
- Sawn into wafers
 - Typically 0.3 mm – 0.5 mm thickness
 - Typically Ø75 mm, Ø100 mm (in R&D)
- Polishing and etching steps
- Chemical cleaning
- Oxidation (diffusion limited flattening)
- Surface implantation or diffusion