Gates and Flip-Flops

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Abstract

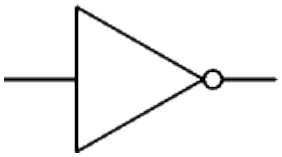
This experiment was carried out to construct (with the exception of the AND and NOT gates) and investigate the outputs of AND, NAND, OR, NOR, XOR and XNOR gates and "J-K master slave flip-flop" circuits when given different inputs using truth tables, 1 indicating a signal and 0 indicating none. Both asynchronous and synchronous counters were then constructed from the J-K master slave flip-flops. The expected logic tables were constructed and the counters worked.

Introduction and Theory

In electronics, logical functions are performed based on incoming signals and pulses in a circuit. Gates and flip-flops are used to perform these functions in what is called a logic circuit. In the logic, called transistor-transistor logic (TTL) signals of a standard size (0V and +5V) are used. The presence of a signal is referred to as a logical 1, or true, while the absence of a signal is referred to as a logical 0, or false. The following gates perform logical operations, outputting either a logical 1 or 0 based on their inputs.

The NOT Gate

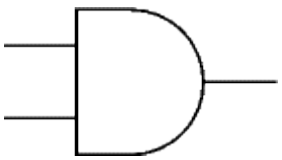
The NOT gate outputs a logical 0 if its input is a logical 1 and outputs a 1 if its input is a 0. The symbol is given.



NOT gate

The AND Gate

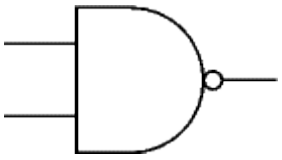
The AND gate outputs a logical 1 if and only if all inputs are a logical 1 and outputs 0 otherwise.



AND gate

The NAND Gate

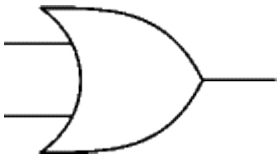
The NAND gate is an AND gate followed by a NOT gate. Therefore, it outputs a logical 0 if and only if all inputs are a logical 1 and outputs 0 otherwise. The symbol is a regular AND gate with a circle at the output.



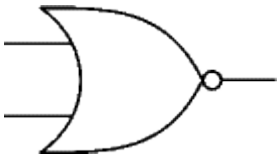
NAND gate

The OR and NOR Gate

The OR gate outputs a logical 1 if at least one input is a logical 1 and a 0 otherwise. The NOR gate outputs 0 where the OR gate would output 1 and 1 where the OR gate would output 0.



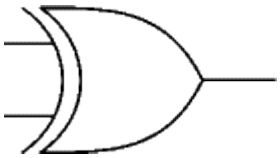
OR gate



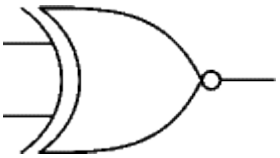
NOR gate

The XOR and XNOR Gate

The XOR gate, or the exclusive OR gate, outputs 1 when one and only one of its inputs are a logical 1 and 0 otherwise. Similarly, the XNOR gate outputs 1 only when all the inputs are the same, and 0 otherwise.



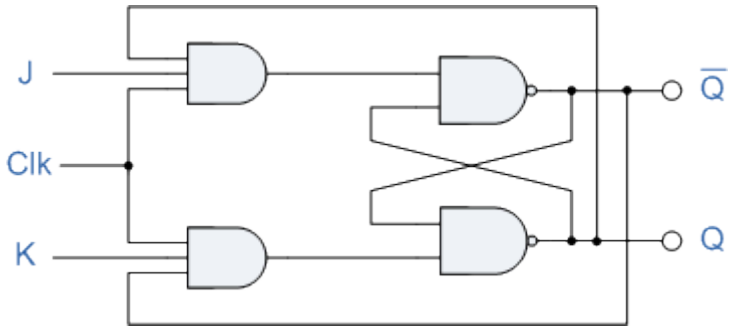
XOR gate



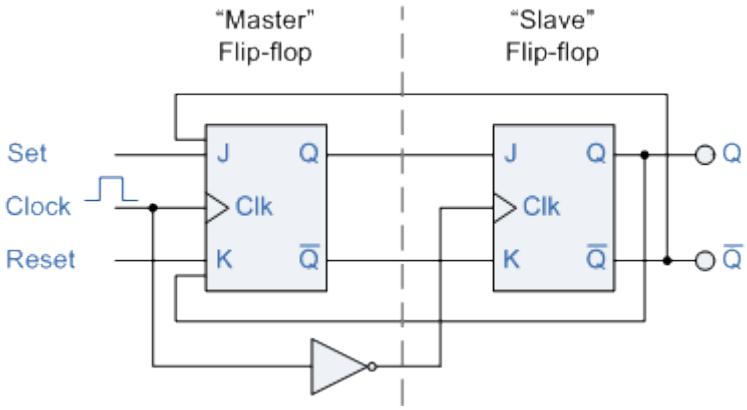
XNOR gate

Flip-Flops

The Flip-Flop remains locked on an output of either 0 or 1 until it is given some sequence of inputs, in which case its output will change. The J-K flip-flop has two outputs, one being the conjugate of the other. The J-K flip-flop is constructed using NAND and NOT gates as shown. The J-K flip-flop outputs reflect the J and K inputs upon the pulse of the clock, but remain locked until then except in the case where J=K=1 where the outputs simply flip upon a pulse. The "clocked J-K master slave flip-flop" was used in this experiment. The output of the "clocked J-K master slave flip-flop" alternates upon a pulse being fed into the clock (a pulse being a sequence of 010 or 101).



J-K flip-flop



Clocked J-K master slave flip-flop

Experimental Method

Care was taken to make sure each gate used was properly connected to the +5V supply and properly grounded in the circuit. The circuits were constructed as instructed and outputs were checked using red LED lights, the light turning on indicating a signal. Inputs came from switches, which could easily be seen to be on or off, and a clock which emitted a pulse on the push of a button or released regular pulses when set.

Results

A NAND gate with 3 inputs was tested and its truth table written out it was found to follow the expected logic. It was also tested with one input disconnected and was found to operate like a 2 input NAND gate.

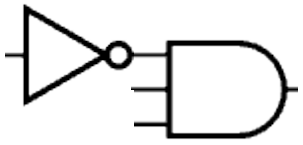
Input A	Input B	Input C	Output
0	0	0	1
1	0	0	1
0	1	0	1
0	0	1	1
1	1	0	1
1	0	1	1
0	1	1	1
1	1	1	0
-	1	1	0
-	1	0	1
-	0	1	1
-	0	0	1

A NOT gate was put after the NAND gate to create an AND gate and the results were tabulated

Input A	Input B	Input C	Output
0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	0
1	0	1	0
0	1	1	0
1	1	1	1

A NOT gate was put before one of the inputs of the AND gate and the inhibit function of this input on the other two inputs was tabulated. It was found that a signal is output only if the inhibit is off and both inputs have a signal.

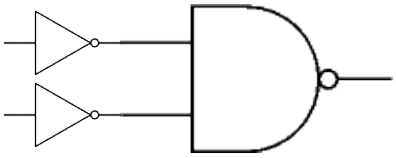
Input A	Input B	Inhibit	Output
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0



Inhibited AND gate

An OR gate was constructed by placing NOT gates in front of the inputs of a NAND gate. The results were tabulated.

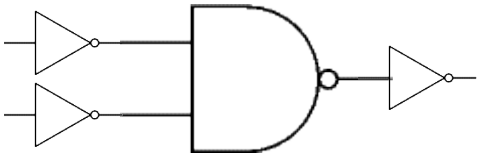
Input A	Input B	Output
0	0	0
1	0	1
0	1	1
1	1	1



The OR gate

The NOT gate was constructed similarly, except an AND gate was used, ie a NOT gate was placed in front of the AND gate.

Input A	Input B	Output
0	0	0
1	0	1
0	1	1
1	1	1



An example OR gate

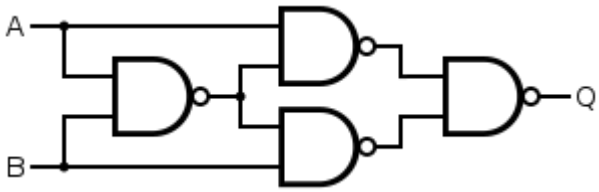
A XOR gate was constructed from NAND gates and its results were tabulated. A XNOR gate was constructed by placing a NOT gate after it.

XOR gate:

Input A	Input B	Output
0	0	0
1	0	1
0	1	1
1	1	0

XNOR gate:

Input A	Input B	Output
0	0	1
1	0	0
0	1	0
1	1	1



An example XOR gate

The J-K master slave flip-flop was constructed as shown in the introduction and the results tabulated.

Input J	Input K	Clock	Q	$\overline{Q}$
0	1	Pulse	0	1
1	0	Pulse	1	0
1	1	Pulse	Alternates	Alternates
0	0	Pulse	Stops	Stops

Several Counters (Scalers) were constructed using the J-K master slave flip-flop. A counter of scale 16 was constructed which counted in binary using the LED lights. An asynchronous counter was first constructed. A scale 10 counter is shown here, but the scale 16 is simply the same without the NAND gate. It was simple to construct counters of any power of two and any other number could be constructed by adding the equivalent binary outputs for the number to the inputs of the NAND gate. In the diagram shown, the conjugate of the clear is shown along with an AND gate. A NAND gate without the conjugate is the same thing.

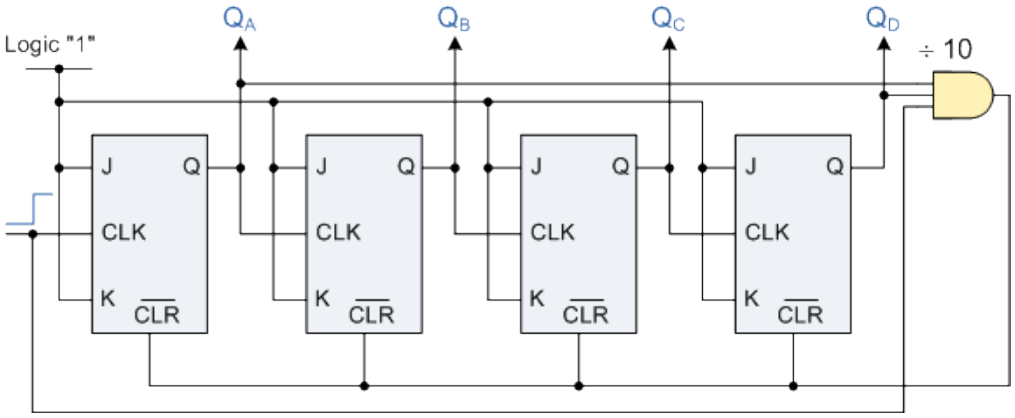
A synchronous counter was then constructed, which is similar to an asynchronous counter, except that all of the flip-flips are pulsed simultaneously.

Scale 16 counter:

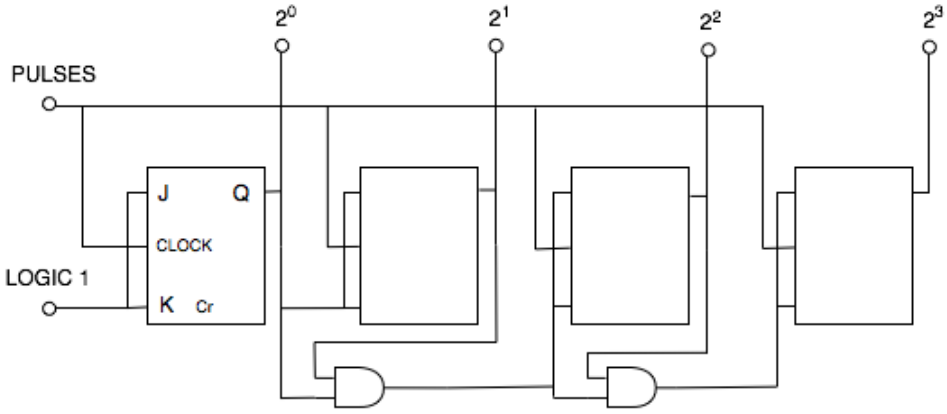
Pulse	2^0	2^1	2^2	2^3
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1
16	0	0	0	0

Scale 10 counter:

Pulse	2^0	2^1	2^2	2^3
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	0	0	0



Scale 10 asynchronous counter



Scale 16 synchronous counter

Discussion and Conclusions

The expected truth table for every gate was verified in this experiment. It was shown that there were several ways to construct each gate from NAND and NOT gates, or even purely from NAND gates since a NOT gate can be constructed from a NAND gate.

The usefulness of J-K master slave flip-flops was shown in the construction of several types of counters.